APPLIED PHYSICS LETTERS **86**, 1 (2005)

High-field-effect-mobility pentacene thin-film transistors with polymethylmetacrylate buffer layer

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(Received 5 January 2005; accepted 7 April 2005)

A thin film of polymethylmetacrylate (PMMA) acting as a buffer layer has been employed in order to fabricate high-quality pentacene thin-film transistors (TFTs), both in bottom contact and top contact configuration. A PMMA buffer layer allows to reduce the interaction between a π-conjugated system of pentacene and the metal or dielectric substrate. We show that a thin PMMA buffer layer improves crystal quality along the metal contacts' boundaries, while still allowing good ohmic contact. Pentacene TFTs, including a PMMA buffer layer, show very high field-effect mobility, $\mu_{FE}=0.65$ and 1.4 cm^2/V s, for bottom and top contact configuration, respectively, and remarkable steep subthreshold region. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1931833]

In recent years there has been a growing interest in organic thin-film transistors (O-TFTs) due to their attractive features such as low cost, low-temperature processing, and mechanical flexibility. O-TFTs have been demonstrated on a variety of substrates, including silicon, glass, or plastics.[1–10] Different organic active layers have been investigated, including pentacene,[1–9] while, as gate insulator, both inorganic [SiO_2 (Refs. 1, 6, and 8), Si_3N_4 (Ref. 9), Al_2O_3 (Ref. 7)] and organic [poly(4-vinylphenol) (PVP) (Ref. 2), polyimide (Ref. 3), parylene (Ref. 10), polyaniline (PANI) (Ref. 4)] dielectrics have been employed. However, the best results at the moment have been obtained for pentacene-based TFTs coupled with both inorganic or organic gate dielectrics. Recent work has shown that using organic materials as gate dielectrics it is possible to obtain very high values for the field-effect mobility,[1,3,10] even higher than those obtained with inorganic gate dielectrics,[1] although inorganic dielectrics provide lower leakage current and lower hysteresis.

The interaction of π-conjugated pentacene with metal contact or gate dielectric surfaces, strongly affects the growth process and determines the morphology of the organic film.[8] In particular, in bottom contact (BC) configuration the polycrystalline pentacene degrades in an amorphous phase along the boundaries of the source and/or drain contacts, decreasing the performance of the devices.[8] It has been demonstrated that the interaction of the π system with interfaces can be decreased covering the surface with a monolayer of octadecyltrichlorosilane (OTS) (Ref. 9), before the deposition of pentacene. Top contact (TC) configuration is normally reported to present better performance and, even without applying a buffer layer, pentacene-TFTs with a field-effect mobility of 3 cm^2/V s, with PVP gate dielectric,[1] and 1 cm^2/Vs, and with polyimide gate dielectric,[3] have been demonstrated. Such high mobility values can be achieved only through an effective control of the gate dielectric-pentacene interface, that allows to reduce defects and grain boundaries. On the other hand, BC configuration is more suitable from an application point of view and in this case the control of the interfaces between pentacene, metal contact, and gate dielectric is required. As mentioned above, the use of OTS as a buffer layer can substantially improve the interface quality, but it can be used only with the dielectrics that contain hydroxy groups (OH), allowing an OTS monolayer to self-assemble on their surfaces.[1] In this work we present, the use of polymethylmetacrylate (PMMA), also known as Plexiglass, as a buffer layer for the fabrication of high-quality polycrystalline pentacene-TFTs. It should be pointed out that PMMA, most often used as electronic resist,[11] is one of the most common plastic material in electronics, thanks to a low-cost, low-temperature process, and high stability, and can be easily processed.

Bottom and top contact devices have been fabricated on heavily doped silicon wafers (acting as gate electrode) with thermal silicon oxide 120-nm thick (gate dielectric). In BC configuration the source and drain gold contacts (30-nm thick) have been defined by optical lithography and wet etching with channel lengths $L=15,25,100,500$ μm and channel width $W=200$ μm. The samples have been annealed at 120 °C for 30 min, cleaned with $HF:H_20=1:80$ for 5 s, and finally covered by spinning with a film of PMMA 950 K annealed at 90 °C for 10 min (thickness about 8 nm). Thermal evaporation of pentacene (Sigma Aldrich 97%) has been performed on the samples with or without the PMMA film, with no extra purification process or substrate heating (evaporation rate about 3 nm/min, vacuum pressure 3×10^{-6} mbar). For TC configuration, gold source and/or drain contacts are evaporated through a shadow mask on top of the pentacene active layer ($L=100$ μm, $W=200$ μm).

AFM measurements show that pentacene film, grown on a SiO_2 surface, exhibit a very good polycrystalline structure, with a characteristic "terrace" structure with a 1.6-nm step. However, the film grown without PMMA becomes amorphous on top of gold contact [Fig. 1(b)] producing a transitional region between the amorphous and polycrystalline structure, located just at the edge of the metal contact [see Fig. 1(b)]. On the contrary, the presence of PMMA produces a continuous polycrystalline structure over both channel and metal contact regions [see Fig. 1(a)]. In addition, AFM measurements on a wide number of samples show that the rms roughness of gold contacts (about 0.6 nm) is not appreciably modified by the presence of the PMMA, indicating that no planarization effects are achieved for the used PMMA thick-

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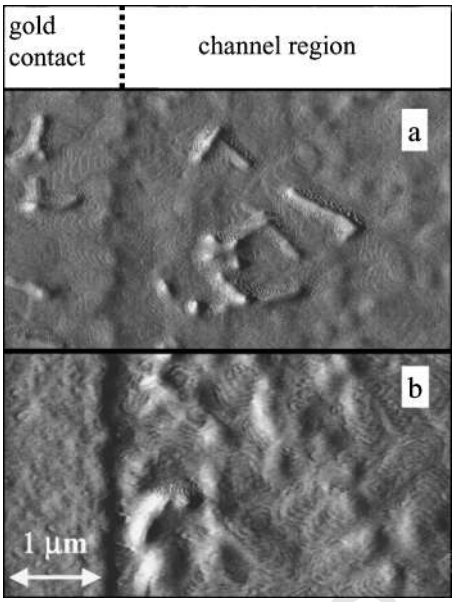

FIG. 1. AFM micrographs of pentacene films, evaporated with (a) and without (b) a PMMA buffer layer, showing the edge between the gold contact (BC configuration) and the TFT channel region.

ness. We then conclude that the role of PMMA is primarily to allow an ordered pentacene growth by inhibiting the direct

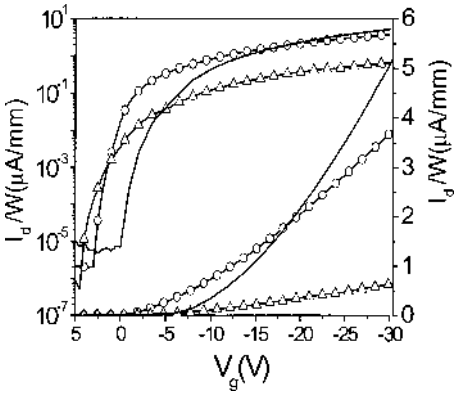

FIG. 2. Transfer characteristics, measured at $V_d=-1$ V, of BC pentacene TFTs with (line+circles) and without (line+triangles) a PMMA buffer layer. Also shown is the characteristic of the TC TFT with PMMA (solid line). Channel length is $L=100$ μm, and channel width is $W=200$ μm for all devices.

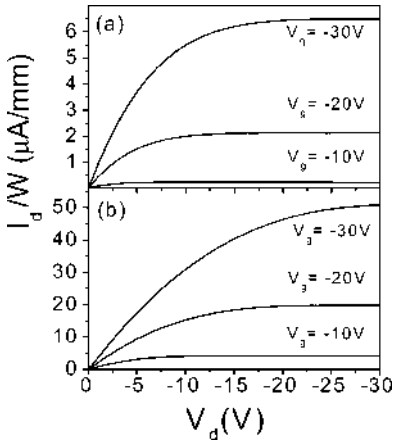

FIG. 3. Output characteristics of BC pentacene TFTs without (a) and with (b) a PMMA buffer layer ($L=100$ μm, $W=200$ μm for all devices).

interaction of the π-conjugated pentacene system with metal or SiO_2 surfaces.

Figure 2 shows the transfer characteristics, measured in vacuum and at $V_d=-1$ V, for devices with or without the PMMA layer ($L=100$ μm, $W=200$ μm). From the experimental data a field-effect mobility $\mu_{FE}=0.65$ (0.13) $cm^2/V\,s$, a subthreshold slope (measured at the onset of subthreshold region) of 0.57 (0.64) V/dec, a threshold voltage Vth$=-6$ (-5) V, and an on/off current ratio of 10^6 (10^6) can be estimated for devices with (without) PMMA. Devices including a PMMA buffer layer show parameters comparable to the best values reported for pentacene-based TFTs (Refs. 1 and 2); the main parameters of a group of representative devices are summarized in Table I. It should be noted that no significant difference can be observed between the mobility values deduced from the saturation regime ($V_d=V_g$) and the value obtained from the linear regime ($V_d=-1$ V). In Fig. 3 the output characteristics with or without PMMA are reported for $L=100$ μm and $W=200$ μm: a good linear behavior at low V_d is observed, suggesting an efficient hole injection from the PMMA/Au contacts.

Figure 4 shows the normalized transconductance versus gate voltage for different $L=15,25,100,500$ μm and, as can be seen, the electrical characteristics do not show the correct scaling for short L, while for $L>25$ μm the correct scaling

TABLE I. Characteristic parameters of the devices measured at $V_{ds}=-1$ V ($W=200$ μm, $d_{ox}=130$ nm, for all devices).

Device	L (μm)	μ (cm^2/V s)	Subthre. slope (V/dec)	V_T (V)	I_{on}/I_{off}
	15	0.25	0.75	−1.0	3×10^6
	25	0.30	0.70	−3.0	3×10^6
BC with	100	0.65	0.57	−6.0	10^6
PMMA	500	0.65	0.61	−8.5	2×10^5
BC without PMMA	100	0.13	0.64	−5.0	10^6
TC with PMMA	100	1.40	0.71	−12	10^6

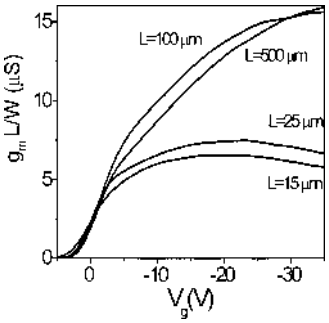

FIG. 4. Normalized transconductance vs gate voltage for different channel lengths $L=15,25,100,500$ μm, for BC pentacene TFT with a PMMA buffer layer.

is observed. This behavior can be caused by the series resistance induced by the PMMA layer, indeed for small value of L, the channel resistance becomes comparable to parasitic resistance related to the transport through the thin PMMA layer. To optimize the PMMA resistance different devices have been fabricated changing the annealing temperature (90/180 °C) and the thickness (8/30 nm) of PMMA. The PMMA resistance increases with the increasing annealing temperature and thickness, and the values used (8 nm, 90 °C) for the device fabrication represent a good compromise to get low series resistance while still having a continuous and homogeneous PMMA film. However, by improving the control of PMMA film thickness, it could be still possible to further decrease the PMMA series resistance by reducing film thickness.

In order to better understand the influence of the series resistance induced by the PMMA layer, devices have been fabricated in both bottom and top contact configuration, codepositing on the two types of substrates the same PMMA and pentacene layers. The transfer characteristics are compared in Fig. 2: the TC device exhibits a $\mu_{FE}=1.4$ cm$^2/Vs$, a subthreshold slope of 0.71 V/dec, and a $V_{th}=-12$ V. We note that the TC device shows a lower current in the subthreshold region, if compared to the BC device, in spite of the PMMA parasitic resistance present in the BC device. This is quite surprising, especially considering that the oxide/PMMA/pentacene interfaces in the channel region of both devices are expected to be the same, as they have been cofabricated, and that, for a given V_g, the same amount of holes should be present in the channels of the two TFTs. We believe that the reduced current in the TC device is due to the effect of the series resistance induced by the vertical transport through the pentacene film and/or the pentacene/Au contact. As the gate voltage is increased in modulus, hole accumulation expands towards the back-channel region, decreasing pentacene vertical resistance as well as contact resistance. In this case, the subthreshold region of TC devices is not controlled by the channel resistance, as also suggested by pentacene-film-thickness dependence of the electrical characteristics.[7] On the contrary, above threshold voltage TC devices show higher on current, if compared to BC devices, suggesting that in this regime the PMMA series resistance limits the on current while the gate-controlled parasitic resistance in the TC devices becomes negligible. This last effect is confirmed by the correct L scaling of the on current (not shown) in the TC devices.

In conclusion, we have fabricated pentacene-TFTs, including a PMMA buffer layer, showing very good performances both in BC and TC configuration. We have demonstrated that a thin PMMA layer can be used in order to obtain good interface quality between pentacene and SiO_2 or Au layers, while still allowing good ohmic contact. In particular, the devices fabricated in the BC and TC configurations exhibit mobility, on/off current ratio, threshold voltage, and subthreshold slope values among the best reported in literature.

This work was supported by the project MICROPOLIS, under the program FIRB funded by Italian Ministry of Education University and Research (MIUR).

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[11]More information on PMMA properties can be found, for instance, on the website http://www.allresist.de