Available online at www.sciencedirect.com
ScienceDirect
Thin Solid Films 515 (2007) 7546–7550
www.elsevier.com/locate/tsf

Aging effects and electrical stability in pentacene thin film transistors

S. Cipolloni, L. Mariucci *, A. Valletta, D. Simeone, F. De Angelis, G. Fortunato

IFN-CNR, Via Cineto Romano 42, 00156, Roma, Italy

Available online 11 January 2007

Abstract

We have studied the transfer characteristic variations induced by aging effects and applied voltage in top contact pentacene thin film transistors (OTFTs) fabricated by using Polymethylmetacrylate buffer layer. The electrical stability of pentacene OTFTs was tested by applying prolonged bias stress (up to 10^4 s) with gate voltage $V_{gstress}=-30$ V and +30 V. The environmental effects were analysed by measuring the degradation of electrical characteristics of OTFT exposed to air. The results have been analysed in terms of trap state model, evaluating the channel conductance using a one-dimensional approach. This allows us to correlate the transfer characteristics variations to changes in localised state distribution.

Keywords: Pentacene; Organic thin film transistors; Electrical stability; Aging effects

1. Introduction

The new opportunities that the use of organic semiconductors offer to device fabrication in the field of large area, low-cost and flexible electronics, have recently increased the research efforts on these materials [1]. Recent results have shown that devices based on some organic semiconductor can be easily compared with those based on amorphous silicon. Indeed, the performance obtained with pentacene-based organic thin film transistors (OTFTs) [2] make possible that OTFTs are used as drivers of organic light emitting diodes in high-resolution active matrix displays [3]. These applications require very reliable devices with relative good on current stability. It has been reported that exposure to air and prolonged applied voltage lead to a decrease of pentacene OTFT performance in terms of field effect reduction, threshold voltage and subthreshold slope variation [4,5]. The observed instability depends upon the detail of device fabrication, as different capping layer and different buffer layers between pentacene and gate dielectric [6,7].

In this work we present an experimental study of the aging effects and electrical stability of high quality pentacene-based OTFTs fabricated by using Polymethylmetacrylate (PMMA) buffer layer.

2. Device fabrication

Devices have been fabricated on heavily doped silicon wafers, acting as gate electrode, thermally oxidised to form the gate dielectric (silicon dioxide thickness of $d_{ox}=80$ and 60 nm), in top contact configuration. Before pentacene deposition, the samples have been spin coated with a film of PMMA 950K (about 5 nm thick) annealed at 90 °C for 10 min. It has been shown that thin PMMA films can be used as buffer layer in order to improve the performance of pentacene OTFTs both in bottom contact and top contact configurations [8]. PMMA buffer layer influences the structure of pentacene grown on SiO_2 [9] modifying the pentacene/dielectric interface. Thermal evaporation of pentacene (Sigma Aldrich, 99% purity) has been performed, by a Radak evaporation source, on the samples without an extra purification process or a substrate heating (evaporation rate about 3 nm/min). Source/drain gold contacts (30 nm thick) are evaporated through a shadow mask on top of the pentacene active layer ($L=100$ μm, $W=200$ μm).

3. Electrical stability

The electrical stability of pentacene OTFTs was tested by applying prolonged gate bias stress (up to 10^4 s) with gate voltage, $V_{gstress}=-30$ V and +30 V, with drain voltage, $V_{ds}=-1$ V. Transfer characteristics, monitored at selected times during the bias-stressing cycle, are shown in Figs. 1 and 2 for

* Corresponding author. Tel.: +39 06 41522229; fax: +39 06 41522220.
E-mail address: mariucci@ifn.cnr.it (L. Mariucci).

0040-6090/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2006.11.064

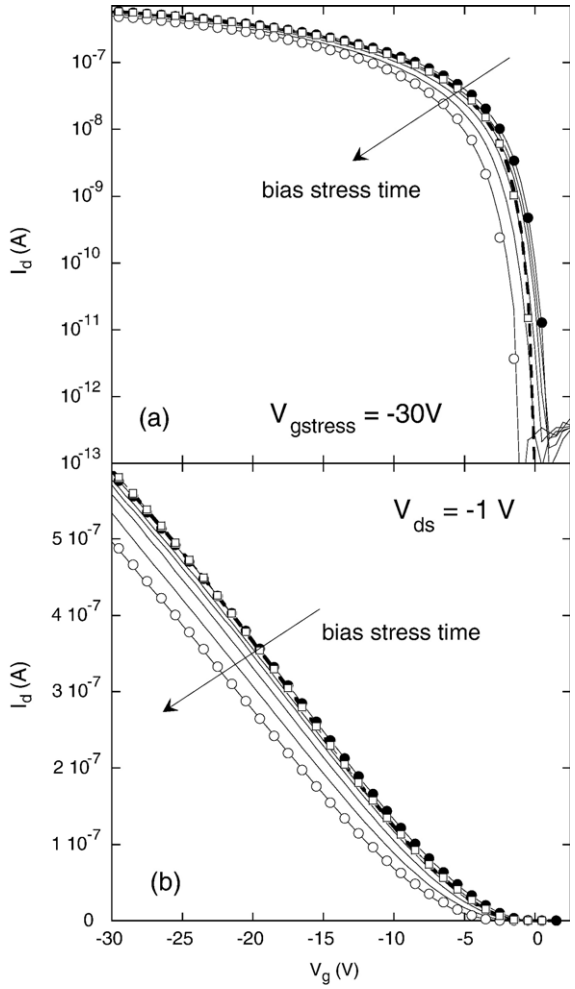

Fig. 1. Experimental transfer characteristics measured at different bias stress times (0–10^4 s) (solid lines) and after 48 h (dashed line). Bias stress condition $V_{gstress}=-30$ V; $V_{ds}=-1$ V. Transfer characteristics, calculated by the trap states model, are also shown, corresponding to unstressed (closed circles), after bias stress (open circles) and recovered device (open squares).

$V_{gstress}=-30$ V and +30 V respectively. Bias stress at $V_g=-30$ V induces an almost rigid shift of transfer characteristics (see Fig. 1), both in linear and subthreshold regimes. Correspondently, field effect mobility (μ_{FE}) and subthreshold slope (S) remain almost unchanged ($\mu_{FE}=.4$ cm^2/Vs and $S=.4$ V/dec), whereas the threshold voltage (V_{th}) monotonically increases, as shown in Fig. 3, from −4.6 V to −7.6 V.

After bias stress the transistor was kept in vacuum at room temperature for 48 h with no applied voltage. The transfer characteristic measured after this period (see Fig. 1) shows a complete recovery of on-current in the linear region, whereas a decrease of subthreshold slope is observed (Fig. 1).

Positive bias stress at $V_g=+30$ produces an almost rigid shift of transfer characteristics toward positive voltages (see Fig. 2). Also in this case, field effect mobility remains almost constant ($\mu_{FE}=.5$ cm^2/Vs) but, contrarily to negative bias stress, subthreshold slope increases from 0.4 V/dec to 0.5 V/dec. However, as in the case of negative bias stress, the most evident phenomenon is the variation of threshold voltage that shows a monotonic shift from −5 V in the unstressed device to −.7 V after 10^4 s (see Fig. 3). The recovery of transfer characteristic after 48 h in vacuum with no voltage applied is not complete (Fig. 2). In particular, a partial reduction of threshold voltage shift was observed, whereas the subthreshold slope does not change relative to bias stress condition.

In analogy with amorphous silicon thin film transistors, the threshold voltage variation can be fitted, for both negative and positive bias stress (see Fig. 3), by a stretched exponential formula:

$$\Delta V_{th}(t) = \Delta V_{\infty}\left\{1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}$$

where $\Delta V_{\infty}=(V_{th}(t=\infty)-V_{th}(t=0))$ is the maximum threshold voltage variation, corresponding to −4.8 V and 5.5 V for negative and positive bias stress, respectively. The fitting parameter β results about .45 for both bias stress, whereas the time constant τ is 11,500 s for $V_{gstress}=-30$ and 2800 s for $V_{gstress}=+30$ V, indicating a faster V_{th} shift for positive bias stress.

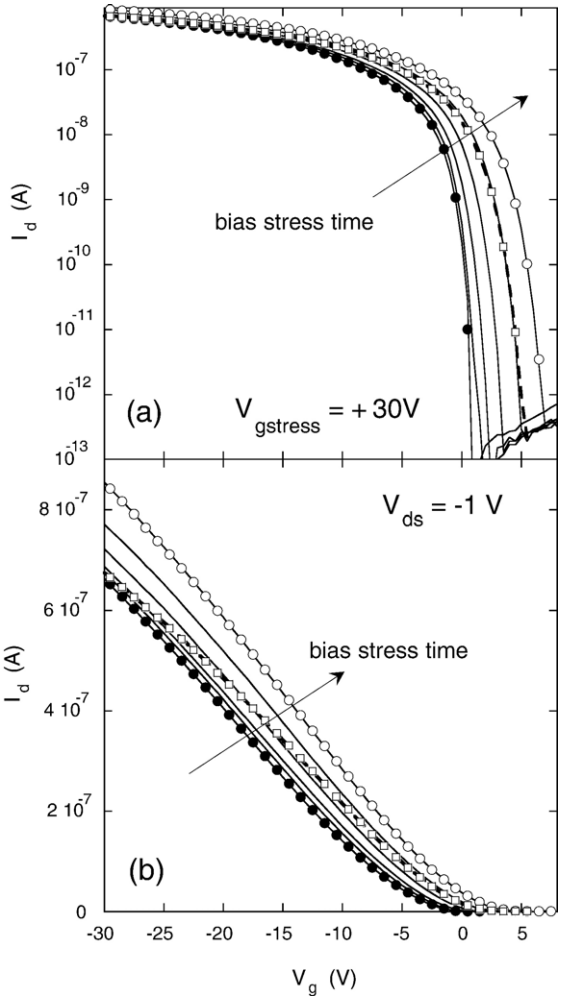

Fig. 2. Experimental transfer characteristics measured at different bias stress times (0–10^4 s) (solid lines) and after 48 h (dashed line). Bias stress condition $V_{gstress}=+30$ V; $V_{ds}=-1$ V. Transfer characteristics, calculated by the trap states model, are also shown, corresponding to unstressed (closed circles), after bias stress (open circles) and recovered device (open squares).

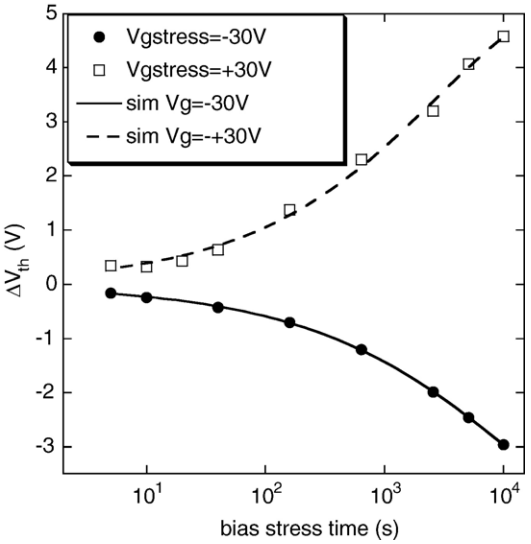

Fig. 3. Threshold voltage variation ($\Delta V_{th}=V_{th}(t)-V_{th}(0)$) for pentacene OTFTs during positive (squares) and negative bias stress. Stretched exponential functions (lines), fitting experimental data, are also shown.

We have analysed the results of bias stress experiments in terms of trap state model. Indeed, it has been shown [10,11] that it is possible to perfectly reproduce the pentacene-based TFT characteristics assuming drift-diffusion transport model and a spatially uniform distribution of localised states (DOS), that includes the contributions of the in-grain and grain boundary defects as well as of the dielectric/pentacene interface defects. DOS can be approximated by the sum of two exponential terms (tail states and deep states): $N(E)=N_t e^{-E/E_t}+N_d e^{-E/E_d}$ [12,13], where E is the energy, measured from the top of the valence band, E_t and E_d are the characteristics energies for the tail-state and deep-state DOS respectively and N_t and N_d are the tail-state and deep-state DOS values at $E=0$, respectively. Transfer characteristics have been computed by evaluating the channel conductance using a one-dimensional approach: the Poisson's equation for the electrostatic potential, ψ, is solved in the direction perpendicular to the active layer surface, x:

$$\frac{d^2\psi}{dx^2}=-\frac{\rho}{\varepsilon_{SC}}.$$

As usual, boundary conditions are imposed on both side of the active layer, thus turning this problem into an implicit boundary value problem: at front interface the solution must satisfy:

$$\frac{V_{gs}-\psi(x=0)}{t_{ox}}\varepsilon_{ox}=-\varepsilon_{SC}\left.\frac{d\psi}{dx}\right|_{x=0},$$

while, at the back interface the electric field must vanish:

$$\left.\frac{d\psi}{dx}\right|_{x=t_{SC}}=0.$$

In order to account for bulk and surface localized states whose energy levels are distributed throughout the organic semiconductor gap, the space charge, ρ, is assumed equal to the sum of the mobile charge, ρ_{free}, that is computed analogously to inorganic semiconductors, and a fixed charge that is given by the sum of two exponential tails of acceptor like states and two exponential tails of donor like states. The contribution to the space charge of a single tail can be written, in the case of acceptor states as:

$$\rho_{trap}^{acc}=\int_{E_v}^{E_c}\frac{1}{1+e^{\frac{E-E_f}{kT}}}N_0 e^{\frac{E-E_c}{E_0}}dE$$

and analogous for donor states. In order to speed up the computation, the integrals are evaluated assuming an approximation for the Fermi function: for E ranging in an interval of $3kT$ around the Fermi level, a third order polynomial approximation is used, while, for E lying outside this interval, an exponential approximation is employed [12]. This leads to an analytical expression that can be directly evaluated. Since in the transfer characteristics the drain bias is low, the Fermi level has been taken equal to $E_f=-V_{ds}/2$, the value that should occur in the mid of the channel. Once discretized, the non-linear

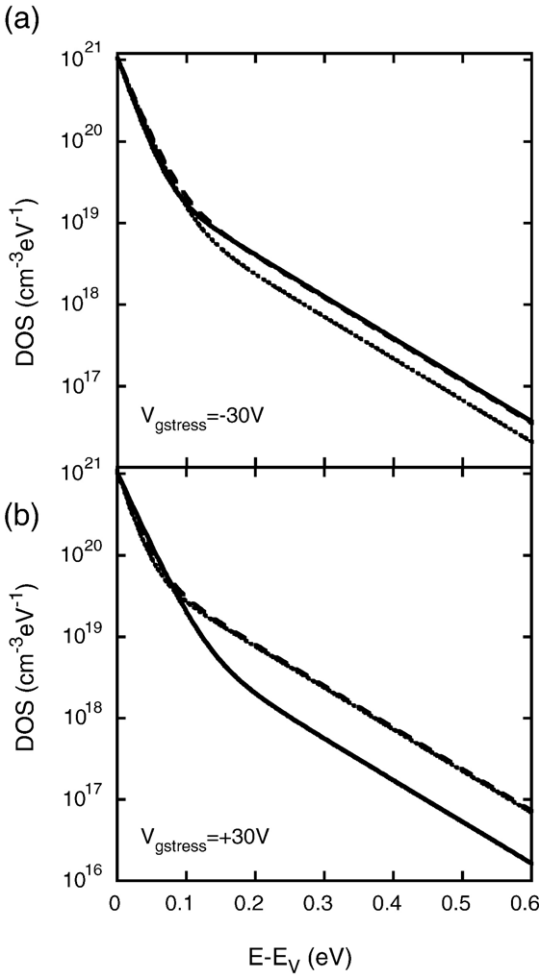

Fig. 4. Density of localized states calculated by fitting transfer characteristics of Figs. 1 (a) and 2 (b), corresponding to negative and positive bias stress, respectively. Solid lines: unstressed devices; dashed lines: after bias stress devices; dot lines: recovered devices.

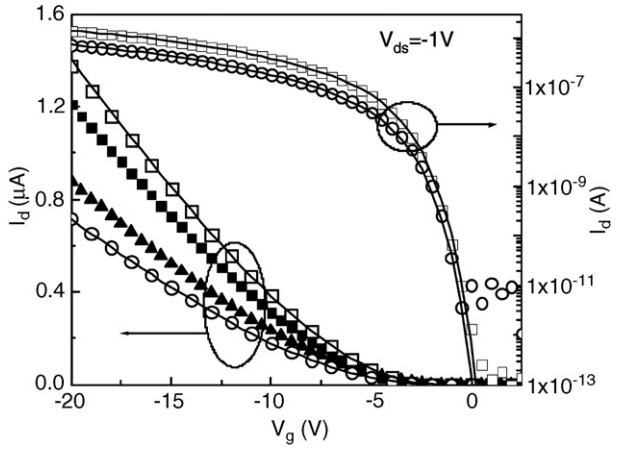

Fig. 5. Experimental transfer characteristics (symbols), measured in vacuum at V_{ds}=−1 V, for as-fabricated devices (open squares) and after 2 (closed squares), 15 (closed triangles) and 40 (open circles) days. (L=100 μm, W=200 μm). Solid lines are the calculated transfer characteristics fitting the as-fabricated and 40-days conditions.

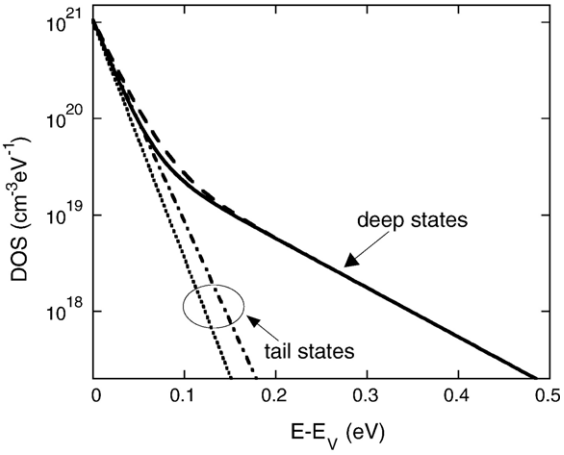

Fig. 7. Density of localized states calculated by fitting transfer characteristics of Fig. 5, corresponding to as-fabricated device (solid line) and the device aged for 40 days (dashed line). Tail states components for as-fabricated (dot) and aged device (dashed–dot) are also shown.

Poisson's equation is iteratively solved using the Newton's method (or relaxation method) and the resulting carrier distribution, along the depth of the channel, is computed. The DOS parameters have been determined by using a least squares approach: the optimisation method used is the Levenberg–Marquardt method [13].

The calculated characteristics are shown in Figs. 1 and 2 for negative and positive bias stress respectively. Fig. 4a shows the calculated DOS for negative bias stress. The localized state distribution does not change during bias stress, whereas, according to the reduction of subthreshold slope in the recovered curve, a reduction of deep states is observed for the transistor measured after 48 h. In addition, simulations confirm that the main effect of negative bias stress is the reduction of flat band voltage from V_{fb}=2.6 V for unstressed device to 0.4 V after 10^4 s. In the case of positive bias stress (Fig. 4b), after bias stress the simulations show an increase of deep states (Fig. 4b) as well an increase of flat band voltage from V_{fb}=2.2 V for unstressed device to 8.7 V after 10^4 s.

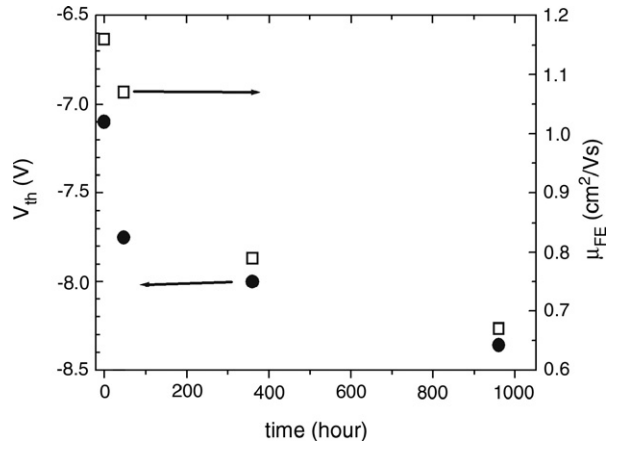

Fig. 6. Threshold voltage and field effect mobility variations during 40 days for a pentacene OTFTs in air. V_{th} and μ_{FE} are calculated from the transfer characteristics shown in Fig. 5.

The mechanism of the observed flat band shift is still not clear. In polymeric thin film transistor threshold voltage variation has been related to "slow" trapping occurring in the disordered area of the polymer film [14]. On the other hand, it has been reported that electric fields induce structural changes of pentacene that can influence charge distribution and carrier motions in a pentacene OTFT [15].

4. Environmental stability

The sample has been exposed to air and light for more than 6 weeks, and has been repeatedly measured, as a function of the exposure time. A representative group of transfer characteristics measured in vacuum at low drain voltage V_d=−1 V, for different aging times, is shown in Fig. 5. As can be seen, the aging phenomenon does not affect the subthreshold region, but it reduces the on-current while the off-current tends to increase with the aging time. The on-current variation is due to the reduction of field effect mobility and the increase of threshold voltage with aging time (see Fig. 6). To calculate the density of localised states we fitted the experimental transfer characteristics by the trap state model above described. As shown in Fig. 5 the calculated characteristics reproduce very well the experimental data. The simulation results confirm that device degradation induced by aging is mainly related to the reduction of carrier mobility. In addition, in the calculated DOS, shown in Fig. 7, it is evident an increase tail-state density for aged devices, whereas deep localized states remain unaffected. This results in a slower turn-on of transfer characteristics and, as a consequence, in the observed increase of threshold voltage in aged device. The tail-state density increase, induced by aging process, could be related to the oxidation of pentacene film, caused by humidity or oxygen contained in air. Indeed, recent experimental results as well as numerical calculation [16,17,6] indicate that adsorbed water and/or oxygen, that induces defects levels near the valence band, are probable origin of the defects in pentacene films oxygen atoms.

5. Conclusions

Bias stress experiments performed on pentacene OTFTs show that the main effect on transfer characteristic is an almost rigid shift toward negative voltages and positive voltages for negative and positive bias stress applied, respectively. In addition, for positive bias stress, a small increase of subthreshold slope has been observed. By using a model with spatially uniform distribution of localised states, we related these variations to changes of flat band voltage and, for positive bias stress, an increase in deep localised states. It has to be noted that the bias stress effects are recovered, at least partially for positive bias stress, after few days. On the contrary, the environmental effects cannot be recovered and produce a reduction of hole mobility and an increase of tail states. These shallow traps can be induced by adsorbed water and/or oxygen.

Acknowledgement

This work was supported by the project MICROPOLIS, under the program FIRB funded by Italian ministry of Education University and Research (MIUR).

References

[1] G. Horowitz, J. Mater. Res. 19 (2004) 1946.
[2] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, W. Weber, J. Appl. Phys. 92 (2002) 5259.
[3] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, T.N. Jackson, Appl. Phys. Lett. 88 (2006) 083502.
[4] C.R. Kagan, A. Afzali, T.O. Graham, Appl. Phys. Lett. 86 (2005) 193505.
[5] D. Knipp, R.A. Street, A. Volkel, J. Ho, J. Appl. Phys. 93 (2003) 3907.
[6] C. Goldmann, D.J. Gundlach, B. Batlogg, Appl. Phys. Lett. 88 (2006) 063501.
[7] S.H. Han, J.H. Kim, J. Jang, S.M. Cho, M.H. Oh, S.H. Lee, D.J. Choo, Appl. Phys. Rev. Lett. 88 (2006) 073519.
[8] F. De Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, Appl. Phys. Lett. 86 (2005) 203505.
[9] J. Puigdollers, C. Voz, I. Martin, A. Orpella, M. Vetter, R. Alcubilla, J. Non-Cryst. Solids 338/340 (2004) 617.
[10] A.R. Volkel, R.A. Street, D. Knipp, Phys. Rev., B 66 (2002) 195336.
[11] F. De Angelis, L. Mariucci, S. Cipolloni, G. Fortunato, J. Non-Cryst. Solids, 352 (2006) 1765.
[12] Y.-T. Tsai, K.-D. Hong, Y.-L. Yuan, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 13 (1994) 725.
[13] S.A. W.H., Teukolsky, W.T. Vetterling, B.P. Flannery, Numerical Recipes in CSecond edition, Cambridge University Press, 1988.
[14] A. Salleo, F. Endicott, R.A. Street, Appl. Phys. Lett. 86 (2005) 263505.
[15] H.L. Cheng, W.Y. Chou, C.W. Kuo, F.C. Tang, Y.W. Wang, Appl. Phys. Lett. 88 (2006) 161918.
[16] O.D. Jurchescu, J. Baas, T.T.M. Palstra, Appl. Phys. Lett. 84 (2004) 3061.
[17] J.E. Northrup, M.L. Chabinye, Phys. Rev., B 68 (2003) 041202(R).