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Effect of active layer thickness on electrical characteristics of pentacene TFTs with PMMA buffer layer

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Abstract

We studied transfer characteristics of pentacene thin film transistors, fabricated by using polymethylmetacrylate (PMMA) buffer layer, in order to evaluate the parasitic series resistance in devices with different active layer thickness (10–80 nm) and contact architectures (top and bottom contacts). For bottom contact TFTs, the highest series resistance ($1.7 \times 10^4\ \Omega$ cm) was found for the thinnest pentacene films, probably related to step coverage problems of the thin pentacene film over the gold contacts. In contrast, for the top contact TFTs, the 10 nm pentacene films had the lowest resistance ($\sim 1.8 \times 10^3\ \Omega$ cm) and the resistance increases to $\sim 8 \times 10^4\ \Omega$ cm for the thicker films. The results can be related to the effect of the series resistance induced by the vertical transport through the pentacene film.

Keywords: Pentacene; Organic thin film transistors; Contact resistance

1. Introduction

Pentacene thin film transistors (TFTs) have recently attracted much interest for large area electronics applications due to its high performance, comparable or even better than amorphous Si TFTs. However, it has been reported that performance of the high mobility pentacene TFTs is strongly affected by parasitic series resistance. Indeed, due to the reduced resistivity of the device channel the contact resistance becomes increasingly important, in particular in short channel devices. It has been shown that series resistance is influenced by contact metal, film thickness, device processing and device architectures [1–8]. Concerning the two typical contact configurations used for organic TFTs, i.e. top contact (TC) and bottom contact (BC) configurations, contact resistances of the order of few $k\,\Omega$ cm have been measured in the case of TC-TFTs [3,4], whereas BC-TFTs exhibit resistance one order of magnitude higher [3,5], probably induced by a more disordered region close to pentacene/metal interface. Parasitic resistance of BC-TFTs is also affected by device process and in particular by different surface treatments before pentacene deposition, as the use of self assembled monolayers or buffer layers [6–8]. We have shown [6] that thin polymethylmetacrylate (PMMA) films can been used as buffer layer in order to improve the performance of pentacene OTFTs both in bottom contact and top contact configurations. On the other hand, in principle, an increase of series resistance in bottom contact configuration can be expected, due to the presence of PMMA layer between pentacene and metal contact. In this work we analyse the transfer characteristics of pentacene thin film transistors, fabricated by using PMMA buffer layer, in order to evaluate the parasitic series resistance in devices with different

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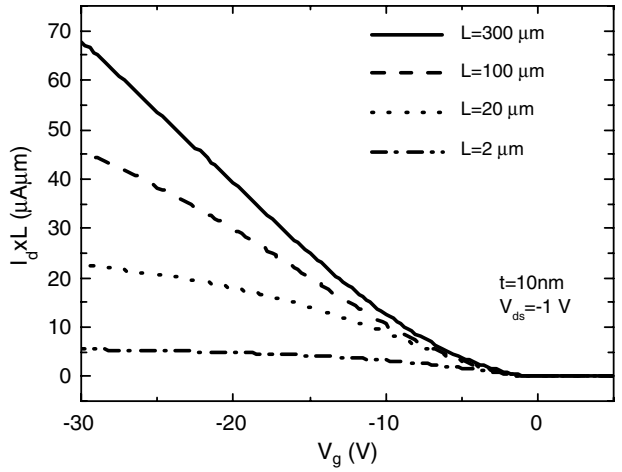

Fig. 1. Low voltage ($V_{ds} = -1$ V) transfer characteristics, normalized to channel length, for pentacene BC-TFTs with 10 nm of pentacene thickness.

active layer thickness (10–80 nm) and contact architecture (top and bottom contacts).

2. Experimental

The devices studied in this work were back gated, using a highly doped-Si substrate as a large area gate, with an 80 nm thermal oxide as the gate dielectric. The active transistor layer was an evaporated film of pentacene in the thickness range $t = 10$–80 nm, which was deposited onto a 5 nm thick alignment layer of PMMA. The source and drain contacts were either formed prior to, or after, the PMMA and pentacene depositions, in order to obtain bottom and top contact TFTs, respectively. These contacts were 20 nm and 30 nm thick layers of gold for the bottom and top contact TFTs, respectively.

The source and drain contacts were defined photolithographically in the bottom contact TFTs, with channel length dimensions on the mask of 2, 4, 10, 20, 100 and 330 μm. For the top contact TFTs, the channel length was defined by shadow evaporation of the gold contacts, giving much longer channel lengths of 30, 100, 300 and 500 μm.

The top contact TFTs were fabricated on the same plates as the bottom contact TFTs and with the same range of pentacene film thickness, so the properties of the pentacene layers should be identical in both cases and the differences can be assumed to be correlated with the different contact structure. It is also worth noting that there should be no step coverage issues for the pentacene films, nor is there an intermediate PMMA layer between the inversion layer and the contact metal.

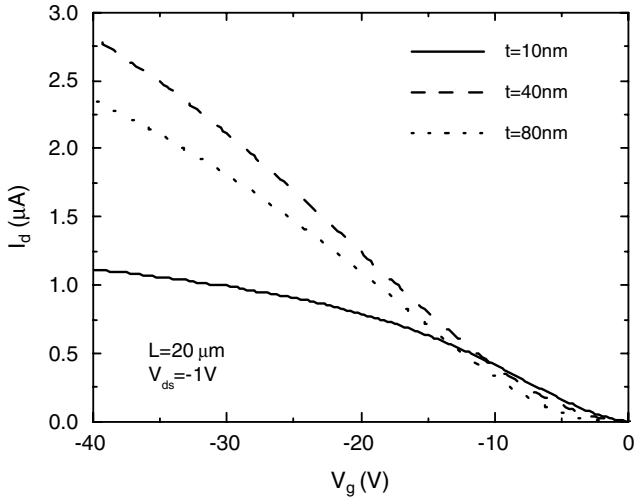

Fig. 2. Transfer characteristics of pentacene BC-TFTs with different pentacene thickness and $L = 20$ μm.

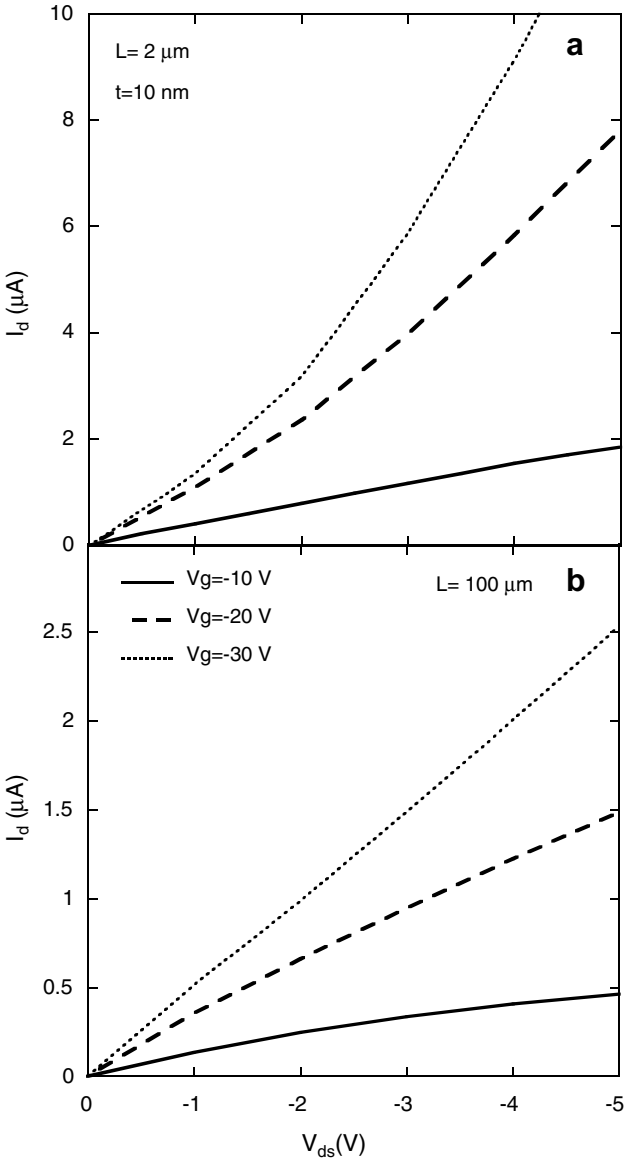

Fig. 3. Output characteristics of pentacene BC-TFTs with $t = 10$ nm and two different channel lengths, $L = 2$ μm (a) and $L = 100$ μm (b), measured at $V_g = -10$, -20 and -30 V.

On the other hand, the current has to flow through the thickness of the film to reach the top contact, and this can introduce additional series resistance.

3. Results and discussion

3.1. Bottom contact TFTs

In Fig. 1 the transfer characteristics, normalized to channel lengths, are shown for bottom contact TFTs with pentacene layer thickness $t = 10$ nm. As can be seen, shorter channel devices exhibit lower normalized drain current, evidencing an increasing influence of parasitic series resistance on device characteristics. Fig. 2 shows the transfer characteristics of BC-TFTs with $L = 100$ μm and different pentacene thickness. Similar characteristics have been measured for thicker devices ($t = 40$ and 80 nm), whereas TFTs with $t = 10$ nm show lower current, mainly related to a non-linear behaviour of the transfer characteristic at high gate voltages. In order to evaluate the parasitic series resistance as a function of gate bias we can consider the following expression:

$$\frac{V_d}{I_d} = \frac{L}{\mu_0 C_{ox} W (V_g - V_t)} + R_s \quad (1)$$

Assuming the parasitic resistance, R_s, to be independent of channel length, gate and drain voltages (ohmic contact) we can calculate R_s from plots of $1/I_d$ vs L. The linearity of the contacts can be evaluated considering the output characteristics at low drain voltages and different gate bias, as shown in Fig. 3. Good low drain voltage linearity is observed for TFTs with channel length $L = 100$ μm, whereas for $L = 2$ μm linearity was only seen for $V_g = -10$ V, and the characteristics were all non-linear by $V_g = -30$ V. TFTs with $L = 20$ μm also start to show non-linearity at $V_g = -30$ V. Taking into account these results, we have calculated the contact resistance for different pentacene thickness, considering devices with channel lengths longer then 2 μm and drain current measured at $V_g = -20$ V. The plot of device total resistance for different channel lengths is shown in Fig. 4. As can be seen, the linearity of the plot is quite good for all the pentacene thickness and, according to Eq. (1), from the intercept values parasitic resistance values can be calculated. BC-TFTs with $t = 40$ and 80 nm show quite similar contact resistances ($R_s = 8$ and 5 kΩ cm, respectively) while for $t = 10$ nm $R_s = 17$ kΩ cm was obtained. The higher R_s-value for the thinnest device can be explained with step coverage problems of the 10 nm thick film over the 20 nm thick gold contacts. It can be pointed out that the R_s values calculated for BC-TFTs with PMMA buffer layer are similar or even better than the R_s obtained for TFTs fabricated by using self-

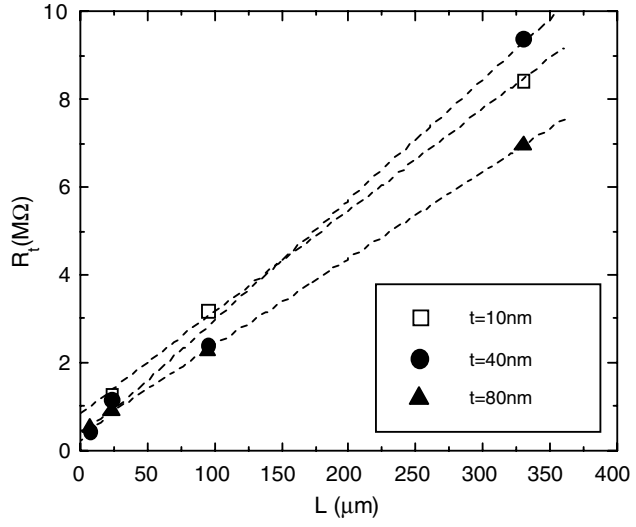

Fig. 4. Total channel resistance vs channel length for pentacene BC-TFTs with different active layer thickness, calculated at $V_g = -20$ V and $V_{ds} = -1$ V.

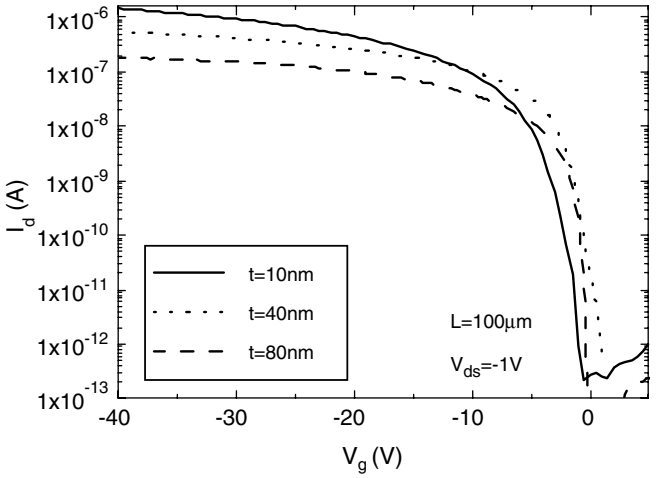

Fig. 5. Transfer characteristics of pentacene TC-TFTs with different pentacene thickness and $L = 100$ μm.

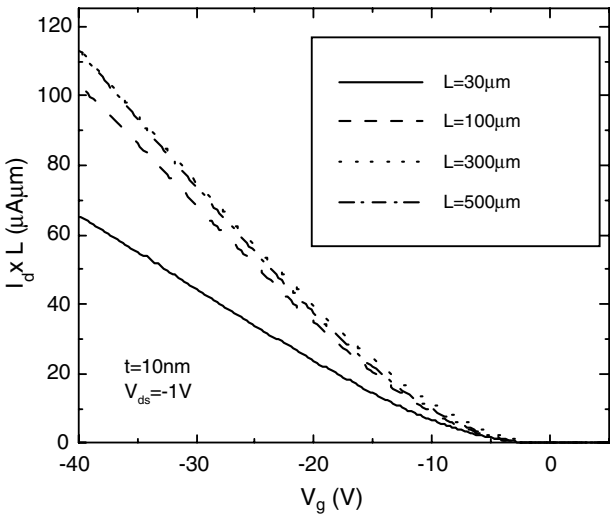

Fig. 6. Transfer characteristics, normalized to channel length, for pentacene TC-TFTs with 10 nm pentacene thickness.

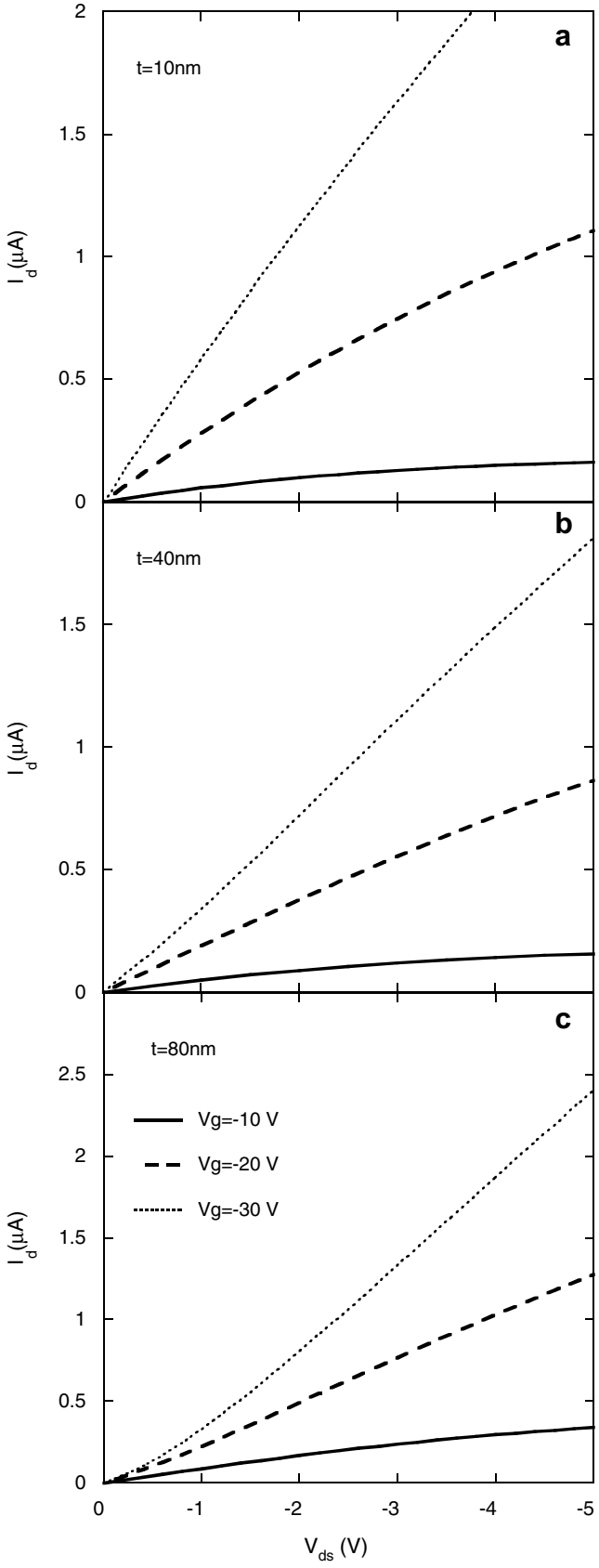

Fig. 7. Output characteristics of pentacene TC-TFTs with $L = 100$ μm and different pentacene thickness, measured at $V_g = -10$, -20 and -30 V.

assembled monolayer (SAM) as alignment layer [3,5]. Considering these contact resistance values, a corrected field effect mobility of about 0.4 cm^2/V s is obtained.

3.2. Top contact TFTs

Fig. 5 shows the low drain voltage ($V_d = -1$ V) transfer characteristics for the $L = 100$ μm top contact TFTs with different pentacene thickness. As can be seen, higher drain current is measured for the thinnest film, suggesting an higher parasitic resistance for thicker films. In addition, thin TC-TFTs seem to be less influenced by parasitic resistance compared to BC-TFTs. Indeed, as shown in Fig. 6, normalised transfer characteristics are affected by contact resistance only for channel lengths $L<100$ μm. As in the case of BC-TFTs, we assessed the contact linearity from the output characteristics (see Fig. 7). The 10 nm thick film shows linear behaviour up to $V_g = -30$ V, whereas linear behaviour is only seen at $V_g = -20$ V and $V_g = -10$ V for $t = 40$ nm and 80 nm, respectively. This behaviour indicates that in TC-TFTs the non-linearity appears to be correlated with the separation of the channel from the contacts. In view of this, the linear regime analysis of Eq. (1) can be correctly performed on the 10 nm and 40 nm thick TFT (at $V_g = -20$ V), whereas for $t = 80$ nm the R_s value obtained should be considered as a rough estimate. From the intercept values of plots in Fig. 8 a parasitic resistance $R_s = 1.8$, 13 and 80 kΩ cm for $t = 10$, 40 and 80 nm, respectively, is obtained.

This thickness dependence of R_s confirms that the main source of series resistance in pentacene TC-TFTs is the vertical current flow through the unaccumulated region between the device channel at the pentacene/dielectric interface and the source/drain contacts.

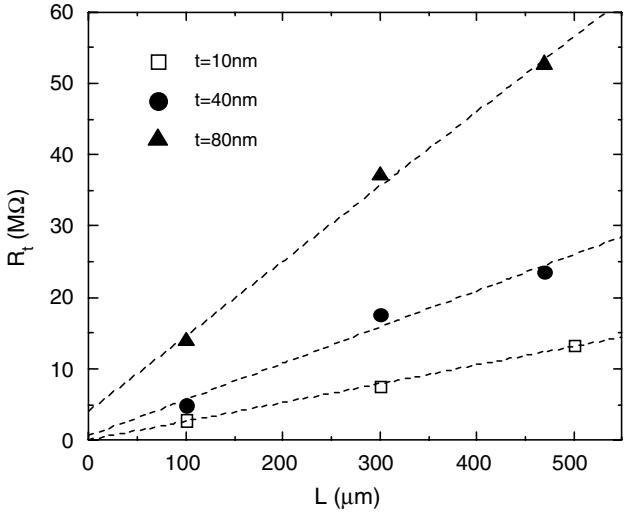

Fig. 8. Total channel resistance vs channel length for pentacene TC-TFTs with different active layer thickness.

4. Conclusion

The series resistance is strongly influenced by contact geometry and film thickness. Better performance and lower series resistance are obtained for TC-TFTs with $t = 10$ nm, but for this contact configuration R_s increases with film thickness. In addition, it has been observed increasing contact non-linearity with increasing film thickness, suggesting that the effect of the series resistance is correlated with the vertical transport through the pentacene film. In contrast, for the BC-TFTs, the highest resistance was found with the thinnest pentacene films of 10 nm, probably induced by step coverage problems of the thin pentacene film over the gold contacts. BC-TFTs with higher film thickness show lower contact resistance as well as less severe contact linearity problems relative to TC configuration. It can be pointed out that the R_s values calculated for BC-TFTs with PMMA buffer layer are comparable with R_s obtained for TFTs fabricated by using different surface treatments (as self-assembled monolayer) before pentacene deposition. This result indicates that the high R_s in BC-TFTs is related to the contact configuration rather than to the specific fabrication process.

References

[1] Gundlach DJ, Zhou L, Nichols JA, Jackson TN, Necliudov PV, Shur MS. J Appl Phys 2006;100:024509.
[2] Lee J, Kim K, Kim JH, Im S, Jung D-Y. Appl Phys Lett 2003;82:9.
[3] Pesavento PV, Puntambekar KP, Frisbie CD, McKenn JC, Ruden PP. J Appl Phys 2006;99:09504.
[4] Necliudov PV, Shur MS, Gundlach DJ, Jackson TN. Solid-State Electron 2003;47:259.
[5] Klauk H, Schmid G, Radlik W, Weber W, Zhou L, Sheraw CD, et al. Solid-State Electron 2003;47:297.
[6] De Angelis F, Cipolloni S, Mariucci L, Fortunato G. Appl Phys Lett 2005;86:203505.
[7] Lyoo KH, Kim B-J, Lee Ca, Jung K-D, Park D-W, Park B-G, et al. IMID/IDMC'06 Digest 2006; 1139
[8] Maeda T, Kato H, Kwakami H. Appl Phys Lett 2006;89:123508.